In re Application of:
Ravindraraj Ramaraju, et al.
Serial No.: 10/646,081
Filed: August 22, 2003
For: DOMINO CIRCUITRY COMPATIBLE STATIC LATCH

September 6, 2006

Art Unit: 2816
Examiner: Kenneth B. Wells
Docket No.: SC12814TC

Certificate of Submission

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September 6, 2006
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Stacie Henyan
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APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313
BOARD OF PATENT APPEALS & INTERFERENCES:

This brief is filed in the matter of the Appeal to the Board of Appeals and Interferences of the rejection of the claims of the above-referenced application for patent.

REAL PARTY IN INTEREST

The present application is wholly assigned to FREESCALE SEMICONDUCTOR, INC., with its headquarters in Austin, Texas.

RELATED APPEALS AND INTERFERENCES

Appellants are unaware of other appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1, 4, 6 and 8-15 are pending. Claims 3, 5, and 16-26 have been canceled. Claims 2 and 7 have been withdrawn.

Claims 1, 4, 6 and 8-15 stand rejected under 35 U.S.C. 102 as being anticipated by US Patent 6,346,836 B1, Wieberneit, and claim 1 stands rejected under US Patent 6,693,476 B1 Lin.

The rejection of claims 1, 4, 6, and 8-15 is being appealed.

STATUS OF AMENDMENTS

An amendment received by the U.S.P.T.O. on June 15, 2006, was filed in response to a final rejection and is believed to have been entered and accurately reflect the pending claims.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is a method claim in which first and second output signals in response to first and second input signals during first and second clock states. Different clock states are described at paragraph [0013]. One example described is that one state is for evaluation and another state is for precharge.

Claim 1 recites a step of providing the first and second input signals at logic states that are complementary during a first clock state. These first and second input signals are shown as being provided as DATA and DATAB in FIG. 1 by domino compatible complementary output circuit 110 to domino-output static latch 120.

Claim 1 further recites a step of providing intermediate signals on first and second nodes at logic states that are complementary in response to the step just described. The first and second nodes are supported as shown in FIG. 2 by the nodes 252 and 254 between transistor 202 and inverter 242 and between transistor 212 and inverter 244, respectively.

Claim 1 further recites a step of providing a first clocked inverter coupled to the first node and the second node. This is supported by transistors 222, 224, and 226. Transistors 222 and 224 provide the inverting function and transistor 226 provides the clocking function. An example is described at paragraph [0022], lines 4 and 5 which states that "if DATA transitions from a low to high, node 252 will transition to a low state."

Claim 1 further recites a step of providing a second clocked inverter coupled to the first node and the second node. This is supported by transistors 232, 234, and 226. Transistors 232 and 234 provide the inverting function and transistor 226 provides the clocking function. An example is described at paragraph [0022], lines 6 and 7, which states, "If DATAB transitions from a low to high, node 254 will transition to a low state."

Claim 1 further recites a step of providing both the first and second input signals at one of the complementary logic states during the second clock state. This is described at paragraph [0020], "While in precharge state 310, the data signals DATA and DATAB ... are held to a logic low..." The precharge state supports the second clock state.

Claim 1 further recites a step of enabling the clock inputs of the first and second clocked inverters in response to a transition from the first clock state to the second clock state resulting in latching the first and second complementary logic states. The support for this operation is described at paragraph [0023], which states, "latch 120 terminates evaluation and initiates latching during latching stage 340 (Figure 3)." The evaluation phase supports the claimed first clock phase. Paragraph [0023} continues by stating, "CLKB transitions to a high state (e.g., at 450 and 455), thereby enabling the cross-coupled inverters 220 and 230 ..." This describes the correlation between the clock signal CLKB and the transition from the first clock state to the second clock state.

Claim 1 concludes with a step of providing the output signals responsive to the first and second intermediate signals. As shown in FIG. 2, inverters 242 and 244 provide output signals DOUT and DOUTB responsive to the intermediate signals present on nodes 252 and 254, respectively.

Independent claim 6 is a method claim in which first and second output signals are provided in response to first and second input signals.

Claim 6 recites the step of providing the first and second input signals at logic states that are complementary. These first and second input signals are shown as being provided as DATA and DATAB signals in FIG. 1 by domino compatible complementary output circuit 110 to domino-output static latch 120.

Claim 6 further recites a step of providing intermediate signals on first and second nodes at logic states that are complementary in response to the step just described. The first and second nodes are supported by the nodes 252 and 254 between transistor 202 and inverter 242 and between transistor 212 and inverter 244, respectively.

Claim 6 further recites a step of providing a first clocked inverter coupled to the first node and the second node. This is supported by transistors 222, 224, and 226. Transistors 222 and 224 provide the inverting function and transistor 226 provides the clocking function. An example is described at paragraph [0022], lines 4 and 5 which states that "if DATA transitions from a low to high, node 252 will transition to a low state."

Claim 6 further recites a step of providing a second clocked inverter coupled to the first node and the second node. This is supported by transistors 232, 234, and 226. Transistors 232 and 234 provide the inverting function and transistor 226 provides the clocking function. An example is described at paragraph [0022], lines 6 and 7, which states, "If DATAB transitions from a low to high, node 254 will transition to a low state."

Claim 6 further recites a step of providing both the first and second input signals at one of the complementary logic states during a precharge phase. This is described at paragraph [0020], "While in precharge state 310, the data signals DATA and DATAB ... are held to a logic low..."

Claim 6 further recites a step of enabling the clock inputs of the first and second clocked inverters in response to entering the precharge phase. The support for this operation is described at paragraph [0023], which states, "latch 120 terminates evaluation and initiates latching during latching stage 340 (Figure 3)." The evaluation phase supports the claimed first clock phase. Paragraph [0023} continues by stating, "CLKB transitions to a high state (e.g., at 450 and 455), thereby enabling the cross-coupled inverters 220 and 230 ..." This describes the correlation between the clock signal CLKB and the transition from the first clock state to the second clock state. At paragraph [0020] it is explicitly stated that "each time the data clock CLK of circuit 100 transitions into a low state (and therefore complementary clock CLKB transitions into a high state ...) latch 120 enters precharge state 310 as shown in FIG. 3."

Claim 6 concludes with a step of providing the output signals responsive to the first and second intermediate signals. As shown in FIG. 2, inverters 242 and 244 provide

output signals DOUT and DOUTB responsive to the intermediate signals present on nodes 252 and 254, respectively.

Independent claim 10 is a circuit claim which has four subparagraphs.

Claim 10 recites a first clocked inverter that receives a first input signal and is enabled by a first clock state. This is supported by transistors 202, 204, and 206. Transistors 202 and 204 provide the inversion and transistor 206 provides the clocking. The first clocked inverter is further characterized as being enabled during the first clock state which is supported by the evaluation phase.

Claim 10 further recites a second clocked inverter that receives a second input signal and is enabled by the first clock state. This is supported by transistors 214, 212, and 208. Transistors 202 and 204 provide the inversion and transistor 206 provides the clocking. The first clock state is supported by the evaluation phase. The first and second clocked inverters are further characterized by the first and second input signals being the same logic state during a second clock state. The second clock state is supported by the precharge state in the same manner as described for claims 1 and 6.

Claim 10 further recites a third clocked inverter that receives the output of the first clocked inverter and is enabled during the second clock state. This is supported by transistors 222, 224, and 226. Transistors 222 and 224 provide the inverting function and transistor 226 provides the clocking function. The third clocked inverter is enabled during the second clock state, which is supported by the precharge state as described for claims 1 and 6.

Claim 10 concludes by reciting a fourth clocked inverter that receives the output of the second clocked inverter and is enabled during the second clock state. This is supported by transistors 232, 234, and 226. Transistors 232 and 234 provide the inverting function and transistor 226 provides the clocking function. The fourth clocked inverter is enabled during the second clock state, which is supported by the precharge state as described for claims 1 and 6. The third and fourth clocked inverters are further characterized as having their inputs and outputs cross-coupled which coupling is supported by FIG. 2.

GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

1) Are claims 1, 4, 6 and 8-15 anticipated under 35 U.S.C. 102 by US Patent 6,346,836 B1 (Wieberneit)?

2) Is claim 1 anticipated under 35 U.S.C. 102 by US Patent 6,693,476 B1 (Lin)?

ARGUMENT

Arguments for Ground 1

Independent Claim 1

Independent claim 1 stands rejected under 35 U.S.C. 102 as being anticipated by Wieberneit.

Wiebernet is deficient because it does not meet the requirement of claim 1 of the step of "providing both the first and second input signals at a predetermined one of the complementary logic states during the second clock state." In the case of Wieberneit, the input signals are always complementary; note inverter S1. One benefit of having the input signals ensured of being at one predetermined logic state during the second clock state is that the input inverters (202, 204, 206 and 212, 214, 208) need only be disabled for that logic state. This allows for having only one clocking transistor for each input inverter as well as using that transistor for actually performing the precharge at the beginning of the evaluation phase. Another way of looking at the same thing is that sufficient disabling of the input clocked inverter can be achieved by only one transistor because the input signals are ensured of being at a particular predetermined logic state during precharge. In this case, transistors 202 and 212 are ensured of being non-conductive because the input to them is a logic low so no clocking transistor is necessary. If complete disabling were required for two input logic states, each inverter would require two transistors for the clocking. Further the particular logic state that is chosen can be chosen to optimize the operation. In the example described the logic low state was chosen for the input signals so that the inputs and outputs of the first and second clocked inverters could be precharged to the logic high state through transistors 206, 204, 208,

and 214 at the beginning of the evaluation phase. Discharging the logic high state is generally faster than charging to the logic high state. Thus by precharging to the logic high state, the response to the input signals is faster because one node will stay at the logic high and the other will discharge to the logic low. This avoids the the situation in which the response to the input signals requires the relatively slower transition from a logic low to a logic high. A logic high to logic low transition is faster, for a given transistor size, because it is achieved with N channel transistors becoming conductive rather than P channel transistors. Although a logic low to logic high transition through an N channel transistor is possible, there are issues concerning the threshold voltage drop across the N channel transistor that require increased complexities such as a parallel P channel transistor or bootstrapping or by compensating for the logic high not achieving the full VDD level. Accordingly, applicants submit that claim 1 is patentably distinct over Wieberneit.

The Examiner stated that the distinction pointed out above was "merely the intended use of the applicant's invention and therefore cannot be relied upon to define over the prior art." The distinction in question relates to the first and second input signals being in the same logic state during the second clock state. Applicants disagree that this distinction from Weiberneit is merely an intended use. It's a feature that is not only specifically required in the claims, it is important to the successful operation of the circuit. The claimed input signals are supported by DATA and DATAB shown in FIG. 1. The second clock state is the time when transistor 226 is active which is the time when the inverters 220 and 230 are providing the latching function. If the input signals were not in the same logic state, a logic low in the actual embodiment disclosed, then one of the input signals would be in the logic high state. Thus, for example, if the DATA signal were a logic high, transistor 202 would be conductive and would be attempting to pull the first node to a logic low which would have the effect of forcing DOUT to a logic high. This would defeat the purpose of the latch which is intended to sustain a particular logic states for DOUT and DOUTB during the second clock state which is supported by what is called, in domino parlance, the precharge phase. The successful operation of latch 120 and thus circuit 100 is dependent upon the claimed operation of the input signals.

Accordingly, applicants believe that the claiming of this feature is material and is not just an intended purpose.

Independent claim 6

The issue is substantially the same as for claim 1. Claim 6 is a method claim which requires "providing the first and second input signals at a predetermined one of the complementary logic states during a precharge phase." Thus the statements relative to claim 1 are applicable to claim 6.

Independent claim 10

Although this claim is a circuit claim instead of a method claim, the issue is substantially the same as for claim 1. The claimed limitation on the circuit, "the first and second input signals are in a same logic state during a second logic state," is still that the input signals have a particular character with respect to the clock phases that interrelated to the circuit operation that is not met by Wieberneit. Applicants' claimed circuit has a functional character that is dependent upon the claimed operation of the input signals. Thus, the statements regarding claim 1 apply to claim 10.

Arguments for Ground 2

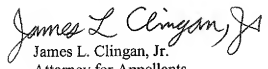
Claim 1,

With regard to Lin, the input signals are either complementary or indeterminate thus do not meet the requirement of "providing the first and second input signals at a predetermined one of the complementary logic states during the second clock phase." The indeterminate state of the input signals of Lin has the same problems as the input signals always being complementary as in Wieberneit. Thus the statements relative to claim 1 regarding Wieberneit apply also to Lin.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the claims of the present application are allowable over the art cited during prosecution.

Respectfully submitted,



James L. Clingan, Jr.
Attorney for Appellants
Reg. No. 30,163
Ph: (512) 996-6839

Claims Appendix

1. (previously presented) A method of providing first and second output signals in response to first and second input signals during first and second clock states, comprising:

providing the first and second input signals at logic states that are complementary during the first clock state;

providing first and second intermediate signals on first and second nodes at logic states that are complementary in response to the step of providing the first and second input signals;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing both the first and second input signals at a predetermined one of the complementary logic states during the second clock state;

enabling the clock inputs of the first and second clocked inverters in response to a transition from the first clock state to the second clock state whereby the first and second intermediate signals at the complementary logic states are latched; and

providing the first and second output signals responsive to the first and second intermediate signals.

2. (withdrawn) The method of claim 1, wherein the first and second clocked inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

3. (Canceled)

4. (original) The method of claim 1, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

5. (Canceled)

6. (Original) A method of providing first and second output signals in response to first and second input signals, comprising:

providing the first and second input signals at complementary logic states;

providing first and second intermediate signals on first and second nodes at the complementary logics states in response to the providing the first and second input signals at the complementary logic states;

providing a first clocked inverter having a signal input coupled to the first node, a signal output coupled to the second node, and a clock input;

providing a second clocked inverter having a signal input coupled to the second node, a signal output coupled to the first node, and a clock input;

providing the first and second input signals at a predetermined one of the complementary logic states during a precharge phase;

enabling the clock inputs of the first and second clocked inverters in response to entering the precharge phase; and

providing the first and second output signals responsive to the first and second intermediate signals.

7. (withdrawn) The method of claim 6, wherein the first and second inverters have second clock inputs, further comprising enabling said second clock inputs in response to providing the first and second input signals at the complementary logic states.

8. (original) The method of claim 6, wherein providing the first and second intermediate signals is achieved by third and fourth clocked inverters responsive to the first and second input signals.

9. (original) The method of claim 8, wherein the third and fourth clocked inverters are characterized as inverting only one of the complementary logic states when the clock inputs are disabled and inverting both logic states when the clock inputs are enabled.

10. (previously presented) A circuit, comprising:

a first clocked inverter having a signal input for receiving a first input signal and an output, wherein the first clocked inverter is enabled during a first clock state;

a second clocked inverter having a signal input for receiving a second input signal complementary to the first input signal during the first clock state and an output, wherein the second clocked inverter is enabled during the first clock state and the first and second input signals are in a same logic state during a second clock state;

a third clocked inverter having a signal input coupled to the output of the first clocked inverter and an output, wherein the third clocked inverter is enabled during the second clock state;

a fourth clocked inverter having a signal input coupled to the output of the second clocked inverter and an output, wherein:

the fourth clocked inverter is enabled during the second clock state; and

the output of the fourth clocked inverter is coupled to the input of the third clocked inverter and the output of the third clocked inverter is coupled to the input of the fourth clocked inverter.

11. (original) The circuit of claim 10 further comprising:

a first inverter having an input coupled to the output of the first clocked inverter and an output for providing a first output signal; and

a second inverter having an input coupled to the output of the second clocked inverter and an output for providing a second output signal.

12. (previously presented) The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to a first power supply terminal, and a second current electrode;

a second transistor having a control electrode coupled for receiving the first input signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for receiving the clock signal, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

13. (previously presented) The circuit of claim 12, wherein the third clocked inverter comprises:

a fourth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second power supply terminal, and a second current electrode coupled to the output of the second clocked inverter;

a fifth transistor having a control electrode coupled to the second current electrode of the first transistor, a first current electrode coupled to the second current electrode of the fourth transistor, and a second current electrode; and

a sixth transistor having a control electrode for receiving the clock signal, a first current electrode coupled to the second current electrode of the fifth transistor, and a second current electrode coupled to the first power supply terminal.

14. (original) The circuit of claim 13, wherein the third and fourth transistors are P channel transistors.

15. (previously presented) The circuit of claim 10, wherein the first clocked inverter comprises:

a first transistor having a control input for receiving the first signal, a first current electrode coupled to a first power supply terminal, and a second current electrode coupled to the signal input of the third clocked inverter;

a second transistor having a control input for receiving the clock signal, a first current electrode coupled to the second current electrode of the first transistor, and a second current electrode; and

a third transistor having a control electrode for being enabled during the first clock state, a first current electrode coupled to the second current electrode of the second transistor, and a second current electrode coupled to a second power supply terminal.

16 – 26 (canceled)

Evidence Appendix

No evidence is submitted in this appendix

Related proceedings Appendix

There are no decisions under this appendix.